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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,226	09/09/2003	Hieu Van Tran	2102397-992830	5736
26379	7590	02/24/2005	EXAMINER	
DLA PIPER RUDNICK GRAY CARY US, LLP			LAM, DAVID	
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E. PALO ALTO, CA 94303-2248			PAPER NUMBER	
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DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/659,226

Applicant(s)

TRAN ET AL.

Examiner

David Lam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-85 is/are pending in the application.
- 4a) Of the above claim(s) 45-51 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 37-44 is/are allowed.
- 6) ☒ Claim(s) 1-4, 16-28, 52, 53, 60-62, 64-66, 68-70, 73-77, 79, 82 and 83 is/are rejected.
- 7) ☒ Claim(s) 5-15, 29-36, 54-59, 63, 67, 71, 72, 78, 80, 81, 84 and 85 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restriction

1. Claims 45-51 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/30/04.

Claim Objections

2. Claims 1, 22 are objected to because of the following informalities:

Claim 1 recited the phrases “a first sensing circuit of memory cells” and “a second sensing circuit of memory cells” are unclear. Examiner does not understand that the first/second sensing circuit detect the selected ones of the first/second plurality of memory cells using a first/second sensing mode content or the first/second sensing circuit detect content of the selected ones of the first/second plurality of memory cells using a first/second sensing mode.

Claim 22 recited the phrase “a sensing circuit memory cells” on amendment page 5, lines 1-3 is unclear. Examiner does not understand that the sensing circuit detect the selected ones of the first/second plurality of memory cells using a first/second sensing mode content or the first/second sensing circuit detect content of the selected ones of the first/second plurality of memory cells using a first/second sensing mode. Appropriate correction is required.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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4. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Abedifard et al. (6,657,913).

Regarding to claims 1-4, Abedifard et al. disclose a data storage comprising: first/second memory array (104, 106) including a first plurality of memory cells; first/second decoder (118, 122) for selecting ones of the first/second plurality of memory cells; first/second sensing circuit for detect the selected ones of the first/second plurality of memory cells, wherein the first and second plurality of memory cells are arranged in segments (400₀₋₃) having first size and second size. *See Figs. 1, 7-8; Cols. 5, 10-11.*

5. Claims 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Fung et al. (6,215,685).

Regarding to claims 16-21, Fung et al. disclose a storage system comprising: a plurality of memory cells (81, CAM); a plurality of tag bit cells (83b), wherein the memory cells are nonvolatile/volatile (RAM, CAM), wherein the tag bits/tag bit cells are single level or multilevel. *See. Figs. 6-11; Cols. 6-9.*

6. Claims 22, 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Nixon (5,819,305).

Regarding to claim 22, Nixon discloses a memory system comprising: a first memory array (50) including a first plurality of memory cells; a first decoder circuit (56) for selecting ones of the plurality of memory cells; a second memory array (60) including a second plurality of memory cells; a second decoder circuit (66) for selecting ones of the second plurality of

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memory cells; a sensing circuit (70, 72, 80) for selecting content of the selected one of the first plurality of memory cells by using first sensing mode, and selecting content of the selected second ones of the second plurality of memory cells by using second sensing mode.

As of claims 25-28, Nixon further discloses wherein the sensing circuit is configurable to switch between the first and second sensing modes, between a high-speed and a low speed sensing mode and multilevel mode and single level sensing mode. *See Figs. 2-4; Cols. 2-6.*

7. Claims 60-62, 64-66 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinkai (6,381,190).

Regarding to claims 60-62, 64-66, Shinkai discloses a data storage system comprising: a plurality of memory arrays (bank a-b), each memory array including a plurality of memory cells for storing content therein, a decoder circuit (14, 15) for selecting ones of the plurality of the memory cells and sensing circuit to select the content of the selected ones of the plurality cells; an interface controller (data control circuit) to perform interface depending on the selected memory array or depending on an external interface; an I/O driver controller (6, 5, 16) to perform an appropriate I/O driver interface depending on the selected memory array or depending on an external interface; and a general purpose memory controller (9). *See. Fig. 2; Cols. 5-8.*

8. Claims 52-53, 82 are rejected under 35 U.S.C. 102(e) as being anticipated by Roohparvar (6,657,899).

Regarding to claims 52-53, Roohparvar disclose a data storage system comprising: a plurality of arrays (104, 106, 108, 110), each memory array including a plurality of memory cells for storing content therein, a decoder circuit (118, 122) for selecting ones of the plurality of memory cells, a sensing circuit to selectively detect content of the selected ones of the plurality of memory cells; a memory controller (200) to perform a first memory operation on a first one of the memory arrays and perform a second memory operation on a second one of the memory arrays concurrently, the first and second ones of the memory arrays storing first and second type of content, respectively, wherein the first and second memory operation are selected from one of program, erase and read. *See. Figs. 1A, 32-33; Cols. 4, 27-28.*

As of to claim 82, Roohparvar disclose a data storage system comprising: a memory (102) comprising a plurality of memory arrays (104, 106, 108, 110), each memory array including a plurality of memory cells for storing content therein; a first one of the memory array executing a first memory operation and a second one of the memory array executing a second operation concurrently, the first and second memory arrays storing first and second type of content, respectively.

9. Claims 77, 79 are rejected under 35 U.S.C. 102(e) as being anticipated by Ha (5,406,519).

Regarding to claims 77, 79, Ha discloses a memory system comprising: an array (11) comprising: a first plurality of memory cells being configurable to a number of memory levels and arranged in a plurality of array sectors, a security key/measure stored for each arrays sector

(storage array, code array); a decoder (4) for selecting one s of the first plurality of memory cells;
a sensing circuit (6) to detect content of the selection ones of the first plurality of memory cells.

See Figs. Figs 2-3; Cols. 2-6.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 23-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Nixon (5,819,305) in view of Abedifard et al. (6,657,913).

As per above discussion, Nixon discloses the claimed invention but lack an inclusion of wherein the first and second plurality of memory cells are arranged in segments and the segments of the first plurality of memory cell are first size and the segment of the second memory cells are a second size. However, Abedifard et al. disclose a plurality of memory arrays (104, 106) including a first/second plurality of memory cells, wherein the first and second plurality of memory cells are arranged in segments (400_{0.3}) having first size and second size. It would having bee obvious to one having ordinary skill in the art at the time of the invention to modify Nixon's arrays by utilizing Abedifard's teaching to provide high-speed access in high-performance memory device. *See Figs. 1, 7-8; Cols. 5, 10-11.*

11. Claims 68-70, 73-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fung et al. (6,215,685).

Regarding to claims 68-70, Fung et al. discloses a storage system comprising: a content addressable memory (30) including a first plurality of multilevel memory cells (10); a selector (22) for selecting ones of the first plurality of memory cells of the content addressable memory; a sensing circuit (25a) to detect content of the selected one of the first plurality of memory cells; a tag bit memory (20) for storing tag bit indicators of content stored in corresponding ones of the plurality of memory cells; a tag bit sensing circuit (25a) to detect a selected tag bit indicator corresponding to selected one of the first plurality of memory cells. *See Figs. 6-7, 11; Cols. 6-9.*

As per above discussion, Fung et al. disclose the claimed invention, but not explicitly disclose an extension decoder circuit for selecting ones of the first plurality of the memory cells of the content addressable memory. However, Fung et al. disclose a selector (22) for selecting ones of the first plurality of memory cells of the content addressable memory. It would have been obvious to one having ordinary skill in the art at the time of the invention of modify by utilizing Fung's selector without alternate the result performance of the device to provide a high-speed, low power consume content addressable memory device.

With regard to claims 73-76, Fung et al. discloses a storage system comprising: an extension array (30) comprising a first plurality of memory cells (10) being configurable to a number of memory levels; an extension selector (22) for selecting ones of the first plurality of memory cells of the content addressable memory; a sensing circuit (25a) to detect content of the selected one of the first plurality of memory cells; a tag bit memory (20) for storing tag bit

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indicators of content stored in corresponding ones of the plurality of memory cells; a tag bit sensing circuit (25a) to detect a selected tag bit indicator corresponding to selected one of the first plurality of memory cells. *See Figs. 6-7, 11; Cols. 6-9.*

As per above discussion, Fung et al. disclose the claimed invention, but not explicitly disclose an extension decoder circuit for selecting ones of the first plurality of the memory cells of the content addressable memory. However, Fung et al. disclose an extension selector (22) for selecting ones of the first plurality of memory cells of the content addressable memory. It would have been obvious to one having ordinary skill in the art at the time of the invention of modify by utilizing Fung's extension selector without alternate the result performance of the device to provide a high-speed, low power consume content addressable memory device.

12. Claim 83 rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar (6,657,899) in view of Choate (4,051,354).

Regarding to claim 83, Roohparvar discloses the claimed as noted above but lack an inclusion of wherein the memory is monolithic. However, Choate discloses a programmable memory comprising a plurality of monolithic arrays (10a-e). It would have been obvious to one having ordinary skill in the art at the time of the invention to form a plurality of monolithic arrays of Roohparvar's memory to provide reliable, efficiency and high-speed semiconductor memory device. *See. Fig. 10; claims 5-6, 53.*

Allowable Subject Matter

13. Claims 5-15, 29-36, 54-59, 63, 67, 71-72, 78, 80-81, 84-85 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is an examiner's statement of reasons for allowance: Claims 37-44 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach: a data storage system comprising: a first sensing circuit, among others as claimed in independent claim 37, to selectively detect content of selected portion of the first plurality of memory cells by using a first sensing mode or a second sensing mode, wherein the first and second sensing modes determined by the selected tag bit corresponding to the selected memory cells.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

February 15, 2005



DAVID LAM
PRIMARY EXAMINER